

INTERNATIONAL STANDARD

ISO/IEC 14576

First edition
1999-12

Information technology – Synchronous split transfer type system bus (STbus) – Logical layer

*Technologies de l'information –
Bus de système de transfert de fente synchrone (STbus) –
Couche logique*

© ISO/IEC 1999

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

ISO/IEC Copyright Office • Case postale 56 • CH-1211 Genève 20 • Switzerland



PRICE CODE

X

For price, see current catalogue

Contents

1. Overview	1
1.1 Scope	1
1.2 Applicability	1
2. Definitions	3
2.1 Explanation of Terms	3
2.2 Notation	5
3. Interface Specifications	6
3.1 Interface Signals	6
4. Bus Operations	11
4.1 Protocol for Basic Operations	11
4.2 Transfer Protocol	16
4.2.1 Bus operation types	16
4.2.2 Command format	16
4.2.3 Transfer sequence	25
4.3 Arbitration	27
4.4 Status Reports	27
4.5 Data Transfer	29
4.5.1 Memory access (write)	29
4.5.2 Memory access (read)	35
4.5.3 Control space access (write)	38
4.5.4 Control space access (read)	40
4.5.5 Message transfer	42
4.5.6 Control register access (write)	44
4.5.7 Control register access (read)	46
4.6 Lock Operations	48
4.7 Cache-related Operations	50
4.7.1 Cache invalidation	50
4.7.2 Retry indication	53
4.7.3 Copyback and steal operations after retry indication	55
4.7.4 Steal inhibit operation	57
4.8 Error Handling	59
4.8.1 Handling errors notified in answer	59
4.8.2 Other error detection	61

5. Cache Coherency Control	62
5.1 Cache Control Methods	62
5.2 Cache Block Attributes	62
5.3 Operations on System Bus	63
5.4 Retry Indication	65
5.5 Steal Operation	66
5.6 Cache Data Management and State Transition	67
5.6.1 Write-through cache	67
5.6.2 Copyback cache	70
5.7 Notes on Memory Access	75
6. Functions for Enhanced Reliability	76
6.1 Redundancy	76
6.2 Detecting Faults	77
6.3 Preventing Faults from Spreading	77
6.4 Supporting Fault Handling and Diagnosis	78
Annex A (informative) Performance (Estimated)	79
Annex B (informative) Return of answer in a lock transfer	80
Annex C (informative) Lock transfer and write back of copyback cache	81

Figures

Figure 1 - STbus Applications	2
Figure 2 - Connection interface between function units (basic pattern)	7
Figure 3 - Concept of bus operation protocol (for 1-cycle or 2-cycle transfer: 8-byte bus width specification, write operation)	11
Figure 4 - Concept of bus operation protocol (for transfer of 3-cycles or more: 8-byte bus width specification, read operation)	13
Figure 5 - Concept of bus operation protocol (for 1-cycle or 2-cycle transfer: 4-byte bus width specification, write operation)	15
Figure 6 - Pipeline operation.....	20
Figure 7 - BCT field.....	21
Figure 8 - RA and byte alignment.....	23
Figure 9 a) - One-word memory write (no-answer transaction)	31
Figure 9 b) - One-word memory write (basic transaction).....	32
Figure 9 c) - n-word memory write (no-answer transaction)	33
Figure 9 d) - n-word memory write (basic transaction)	34
Figure 10 a) - One-word memory read.....	36
Figure 10 b) - n-word memory read	37
Figure 11 - n-word write: control space access.....	39
Figure 12 - n-word read: control space access	41
Figure 13 - n-word message transfer.....	43
Figure 14 - One-word write: control register access	45
Figure 15 - One-word read: control register access	47
Figure 16 - Bus lock transfer.....	49
Figure 17 - Cache invalidation.....	52
Figure 18 - Retry indication	54
Figure 19 - Copyback and steal operations after retry indication	56
Figure 20 - Steal inhibit operation	58
Figure 21 - Error report in answer transaction when DUT detects error	60
Figure 22 - When function unit (0#) detects time out.....	61
Figure 23 - Relation between CPU operation and commands on system bus	64
Figure 24 - STbus write-through cache coherency control protocol.....	69
Figure 25 - STbus copyback cache coherency control protocol	74
Figure A.1 - STbus performance (in 8-byte bus width and 32-bit addressing mode)....	79
Figure B.1 - Example of dead lock problem	80
Figure C.1 - Example of lock transfer to EM cache data.....	81

Tables

Table 1 - Basic Interface Signals (function unit interfaces other than bus handler)	6
Table 2 - Optional Interface Signals (function unit interfaces other than bus handler) ...	6
Table 3 - Command Format for Information Transfer Bus.....	17
Table 4 - OPT Code Definitions	18
Table 5 - M Bit Definition	19
Table 6 - Message Sequence	22
Table 7 - Answer Code Definition	28
Table 8 - System Bus Command Types.....	63
Table 9 - Semantics of Discrepancy between Base and Spare Signals	76

INFORMATION TECHNOLOGY –
SYNCHRONOUS SPLIT TRANSFER TYPE
SYSTEM BUS (STbus) –
LOGICAL LAYER

FOREWORD

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 14576 was prepared by subcommittee 26: Microprocessor systems, of ISO/IEC joint technical committee 1: Information technology.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 3.

Annexes A, B and C are for information only.

INFORMATION TECHNOLOGY –
SYNCHRONOUS SPLIT TRANSFER TYPE
SYSTEM BUS (STbus) –
LOGICAL LAYER

1. Overview

1.1 Scope

This International Standard specifies the logical specifications of STbus which is a high-performance and highly reliable system bus. STbus adopts a synchronous transfer method with a high-speed clock and a split transfer method enabling to minimize bus holding time during one bus operation and to use a bus efficiently.

The contents given in this specifications are as follows:

- a) System bus interface signal provisions;
- b) Bus operations and transfer protocol for each bus operation;
- c) Copyback cache coherency control for maintaining consistency between a shared memory and a cache memory of each processor in a multiprocessor system;
- d) Fault detection function using parity check and duplex configuration for control signals.