INTERNATIONAL STANDARD

ISO/IEC 14576

First edition
1999-12

Information technology – Synchronous split transfer type system bus (STbus) – Logical layer

Technologies de l'information –
Bus de système de transfert de fente synchrone (STbus) –
Couche logique

PRICE CODE X

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FOREWORD

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 14576 was prepared by subcommittee 26: Microprocessor systems, of ISO/IEC joint technical committee 1: Information technology.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 3.

Annexes A, B and C are for information only.

INFORMATION TECHNOLOGY –

SYNCHRONOUS SPLIT TRANSFER TYPE SYSTEM BUS (STbus) –

LOGICAL LAYER

1. Overview

1.1 Scope

This International Standard specifies the logical specifications of STbus which is a high-performance and highly reliable system bus. STbus adopts a synchronous transfer method with a high-speed clock and a split transfer method enabling to minimize bus holding time during one bus operation and to use a bus efficiently.

The contents given in this specifications are as follows:

a) System bus interface signal provisions;

b) Bus operations and transfer protocol for each bus operation;

c) Copyback cache coherency control for maintaining consistency between a shared memory and a cache memory of each processor in a multiprocessor system;

d) Fault detection function using parity check and duplex configuration for control signals.